NEC

Customer Notification

VR4133™

64-bit Microprocessor

Operating Precautions

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(A) Table of Operating Precautions

No.	Outline		μPD30133				
		Rev.	1.1	1.2	1.3	1.4	1.5
		Rank Note	I,K	E	P	X	L
1	Simultaneous locking of cache lines with the same index		✗	✗	✗	✗	✗
2	Reception of non IEEE802.3 conformant packages		✗	✗	✗	✗	✗
3	Register content in Ether0/1 blocks		✗	✗	✓	✓	✓
4	Read access from external PCI master		✗	✗	✗	✗	✗
5	Write access to external I/O area		✗	✗	✗	✓	✓
6	Branch delay slot of JAL(X) instruction in MIPS16 mode		✗	✗	✗	✗	✗
7	Disconnect at the end of PCI burst cycle		✗	✗	✗	✗	✗
8	Ethernet: receive short packet		✗	✗	✗	✗	✗
9	Ethernet: excessive data transfer into memory		✗	✗	✗	✗	✗
10	Ethernet: transmit short packet		✗	✗	✗	✗	✗
11	Usage PCI and Ether/CEU/BCU/CSI (using DMA mode) simultaneously		✗	✗	✗	✗	✓
12	Bus arbitration of Internal Bus Arbiter		✗	✗	✗	✗	✓
13	XX-Bit of CP0 status register		✗	✗	✗	✗	✗
14	PCI DMA function		✓	✓	✓	✓	✗

✓ : Not applicable
✗ : applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(B) Description of Operating Precautions

No. 1	Simultaneous locking of cache lines with the same index (Specification change notice)
	Details Simultaneous locking of two cache lines with the same index (i.e. in both cache ways) is prohibited.

No. 2	Reception of non IEEE802.3 conformant packages (Specification change notice)
	Details In case of the reception of a non-IEEE802.3 conformant 18-Byte length Ethernet packet, the internal flow control logic, statistic counter and receive status indicator may no longer work properly. To avoid this situation, control Ethernet reception as follows: (1) Check the FTTYP(27:25) bits of the receive descriptor. If the FTTYP descriptor indicates a control frame or a pause control frame, check the frame type additionally by inspecting the Length/Type field of the Ethernet frame. If this is inconsistent with the content of the FTTYP bits, ignore the FTTYP bits. (2) Additionally the following statistics counters must be adjusted based on the content of the Length/Type field: RXCFC0/1 (0x0f00 1554/1854) RXPFC0/1 (0x0f00 1558/1858) RXUOC0/1 (0x0f00 155c/185c) (3) Flow control must be stopped by setting the RXCF bit in the MACC10/1 registers (0x0f00 1400/1700) to 0y0.

No. 3	Register content in Ether0/1 blocks (Direction of usage)
	Details When burst cycles occur on the internal bus, the content of registers in the Ether0/1 blocks can be changed accidentally, because data information is mistaken as address. To avoid this, the following countermeasures must be taken: (1) The data cache must not be used. (2) The processor must be run in 32-bit mode. (3) The processor must be operated in user- or supervisor mode. (4) The DTBS(1:0) bits in the XMT_CFGR0/1 registers (0x0f00 1600/1900) must be set to 0y00.

No. 4	Read access from external PCI master (Specification change notice)
	Details In case that an external PCI master tries to read data from VR4133 memory via PCI DMA, VR4133 may respond with wrong read data. To avoid this situation, one of the following countermeasures must be taken: (1) Do not use PCI DMA (memory -> PCI). (2) If PCI DMA is used, don't use an external PCI master, that issues read requests to VR4133.

No. 5	Write access to external I/O area (Direction of usage)

Details

A write cycle to external I/O or Flash area after

- a CPU read/write access to a BCU-managed registers[Note]
- or a CPU I/O read after a bus hold
- or a DMA I/O read after a bus hold
- or a Flash memory read

may drive the wrong write data. To avoid this situation, one of the following workarounds must be implemented:

(1) execute a dummy register access to a **non**-BCU-managed register[Note]
(2) execute a dummy external I/O write or Flash write before the actually intended external write

Note: BCU-managed registers are all registers except

SCU registers	`0x0f001000 – 0x0f001009`
SDRAMU registers	`0x0f000400 – 0x0f000409`
PCIU registers	`0x0f000c00 – 0x0f000d43`
ETHER registers	`0x0f001400 – 0x0f00193f`
CEU registers	`0x0f000e00 – 0x0f000e7f`

No. 6	Branch delay slot of JAL(X) instruction in MIPS16 mode (Specification change notice)

Details

A load of PC relative instruction must not be placed in the delay slot of a JAL(X) instruction in MIPS16 mode. Therefore one of the following countermeasures must be taken:

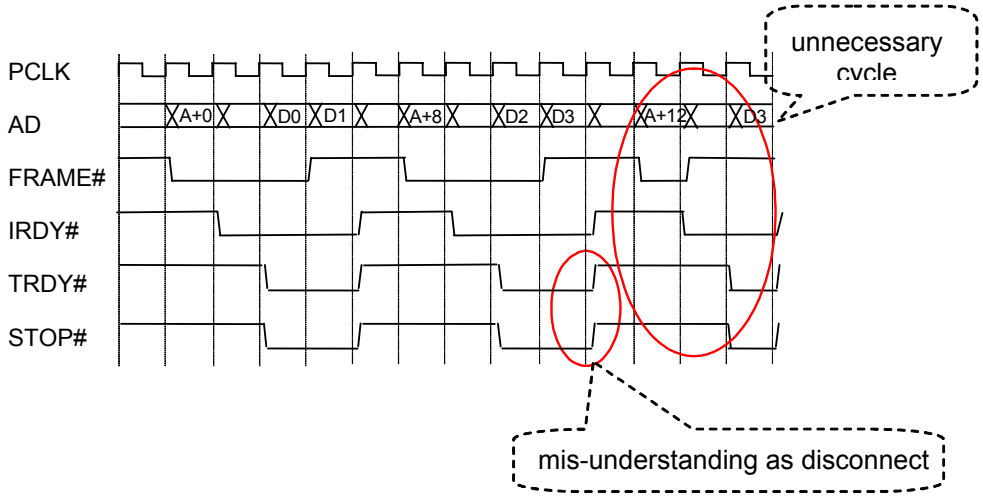
(1) Do not locate a load of PC relative instruction in the delay slot of a JAL(X) instruction in MIPS16 mode.
(2) Do not use JAL(X) instructions in MIPS16 mode; use JAL(X) in native mode instead.

As implementing these countermeasures requires changes in the compilers, MIPS16 will be deleted from the VR4133 specification.

No. 7	Disconnect at the end of PCI burst cycle (Specification change notice)

Details

The last transfer of a PCI burst cycle is regarded as a disconnect cycle by VR4133, if STOP# and TRDY# are both asserted during the last-but-one data cycle, as shown in the following figure:



D0 ,D1,D2 are burst data; D3 is last burst data and D2 is last-but-one burst data. TRDY# and IRDY# are both asserted during D2 and D3. So data transfer of D2 and D3 is finished. But because of this restriction, VR4133 mis-interpreting data phase as if it is disconnected at D2. Therefore D3 cycle is performed again.

Therefore one of the following workarounds must be implemented:

(1) Do not use PCI-DMA function.
(2) Do not use LD and SD instructions and do not locate PCI memory and I/O areas in cached memory region of the CPU, so that burst cycles as shown above are not generated.

No. 8	Ethernet: receive short packet (Documentation errata)

Details

The packet size of VLAN is designed for minimum 68 bytes length, but this is not described in user's manual.
If a VLAN packet is received with a length of 64-67-byte (less than 68 byte), VR4133 will be judged it as a short packet, and a packet will be discarded.

Using a packet with a length of less than 68 bytes can be realized by the following method:

Set a 'special value' into VLTP (15:0) of VLTP0/1 (0x0f001464 / 0x0f001764) register. The 'special value' has not to be a VLAN type, which you want to receive. The data can be received as a usual packet, and judged as a VLAN packet by software. In this case, following items are different from usual VLAN procedure.

(1) All the VLAN packets recognized by the TYPE field of receiving descriptor status are described as normal packets.
(2) The statistics counter R64C0/1, R127C0/1, R255C0/1, R511C0/1, R1KC 0/1 and RMAXC0/1 count normal packets.

No. 9	Ethernet: excessive data transfer into memory (Direction of usage)

Details

If two or more packets are received continuously, excessive data may be written at the end of a packet. The length of excessive data depends on the value of the DRBS0/1 bits of register RCV_CFGR0/1 (0x0f00 1618 / 0x0f00 1918) and becomes up to [burst length -1].

Therefore one of the following workarounds must be implemented:

(1) Set up burst size as 1 word (4 bytes) by RCV_CFGR0/1 (0x0f00 1618 / 0x0f00 1918).

(2) Allocate the size of the receiving buffer on a memory as [receiving maximum packet length] + [burst size - 1].

No. 10	Ethernet: transmit short packet (Direction of usage)

Details

If following two conditions are both satisfied, the internal DMA controller reads DMA buffer at the same address repeatedly and the ether MAC misunderstands it as a jumbo-frame and a transmit abort may occur, though the length of actual transmitted packet is shorter than the setting of LMAX0/1 (0x0f001414 / 0x0f001714) register:

(1) The length of transmitted packet (indicated by SIZE[15:0]) is longer than the setting of DTBS bit of XMT_CFGR0/1(0x0f001600 / 0x0f001900) register and the packet length is less than 32 bytes; or the burst size set by the DTBS bit is 8 words (32 bytes) and the descriptor buffer size is 30 or 31 bytes.

(2) The physical buffer address pointer, which is indicated by transmit descriptor is not word-aligned.

Therefore one of the following workarounds must be implemented:

(1) Set 8-word (32bytes) to the burst size of DTBS in XMT_CFGR0/1(0x0f001600 / 0x0f001900). If the descriptor size is 30 or 31 bytes, set a word-aligned address as the physical address value indicated by the transmit descriptor.

(2) Set word-aligned address to the physical buffer address pointer, which is indicated by transmits descriptor.

(3) Set 32-bytes or more to SIZE[15:0] of transmit descriptor.

No. 11	Usage PCI and Ether/CEU/BCU/CSI (using DMA mode) simultaneously (Direction of usage)

Details

Using PCI and Ether / CEU / BCU / CSI (using DMA mode) simultaneously may occur a hang-up, if following 3 conditions are all satisfied:

(1) CPU reads PCI bus or PCIU register (0x0f000cxx / 0x0f000dxx).
(2) External PCI master reads or writes SDRAM connected to VR4133.
(3) When using DMA between Ether/CEU/external I/O(ROM)/CSI and SDRAM.

To avoid this situation, the following workaround must be implemented:

Set 1 to CONFIG_DONE bit of PCIENREG (0x0f000c34) before and after PCI read from.

```
Example:
      LW   t0,0xAF00
      SW   zero,0x0C34(t0)    /* CONFIG_DONE <-0  */
      LW   zero,0x0000(t0)    /* read back CONFIG_DONE bit */
      LW   rx,0(ry)           /* PCI bus or PCIU read from CPU  */
      LI   t1,4
      SW   t1,0x0C34(t0)      /* CONFIG_DONE <- 1 */
```

No. 12	Bus arbitration of Internal Bus Arbiter (Direction of usage)

Details

If an internal bus request occurs from Ethernet controller and another bus master such as PCI / BCU / CSI(using DMA) / CEU / CPU / or another Ethernet controller, the internal bus arbiter may ignore bus arbitration setting of SCUARBITSELREG and gives bus priority to Ethernet controller continuously.
To prevent this situation use following setting:

DRBS0 of RCV_CFGR0/1(0x0f001618/0x0f001918) = 1 and
DRBS1 of RCV_CFGR0/1(0x0f001618/0x0f001918) = 0.

This setting selects a 2 words burst size. In this case the internal bus arbiter can arbitrate to other bus master as well.

No. 13	XX-Bit of CP0 status register (Direction of usage)

Details

The XX-Bit (bit 31) of the CP0 status register does only affect LLD and SCD instructions in 32-bit supervisor mode and 32-bit user mode. These instructions cause in user or supervisor mode a reserved instruction exception, if XX-Bit=0. LL instruction, SC instruction LLD instruction (64-bit mode only) and SCD instruction (64-bit mode only) do not cause a reserved instruction exception in any case.
This description will be added within the documentation of the VR4133.

No. 14	PCI DMA function (Specification change notice)

Details

The VR4133 PCIU's DMA function (VR4133 operates as PCI master and performs DMA transfer between memory and external PCI device) can not longer be used.

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	April 2004	U16551EJ2V0DS00	VR4133 Preliminary Data Sheet
2	February 2004	U16620EJ3V0UM00	VR4133 User Manual

(D) Revision History

Item	Date published	Document No.	Comment
1	October 2003	TPS-HE-B-6009-1	1st release
2	January 2004	TPS-HE-B-6009-2	Added item 8 to 12
3	May 2004	TPS-HE-B-6009-3	Modified item 10
4	June 2004	TPS-HE-B-6009-4	Added item 13 and 14